A CMOS Temperature Sensor With a Voltage-Calibrated Inaccuracy of ±0.15°C (3σ) From −55°C to 125°C

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***Abstract*—This paper describes the design of a low power, energy-efficient CMOS smart temperature sensor intended for RFID temperature sensing. The BJT-based sensor employs an energy-efficient 2nd-order zoom ADC, which combines a coarse 5-bit SAR conversion with a fine 10-bit ΔΣ conversion. Moreover, a new integration scheme is proposed that halves the conversion time, while requiring no extra supply current. To meet the stringent cost constraints on RFID tags, a fast voltage calibration technique is used, which can be carried out in only 200 msec. After batch calibration and an individual room-temperature calibration, the sensor achieves an inaccuracy of $\pm 0.15°C$ (3σ) from $-55°C$ to $125°C$. Over the same range, devices from a second lot achieved an inaccuracy of $\pm 0.25°C$ (3σ) in both ceramic and plastic packages. The sensor occupies 0.08 mm^2 in a 0.16 μm CMOS process, draws 3.4 μA from a 1.5 V to 2 V supply, and achieves a resolution of 20 mK in a conversion time of 5.3 msec. This corresponds to a minimum energy dissipation of 27 nJ per conversion.**

***Index Terms*—Calibration, SAR, sigma-delta modulation, smart sensors, temperature sensor, trimming.**

I. Introduction

COMBINING integrated temperature sensors with Radio Frequency Identification (RFID) tags opens up a wide range of applications e.g. in environmental monitoring, the monitoring of perishable goods and in implantable medical devices. Depending on their source of energy, RFID tags can be classified into passive and active tags. While passive tags scavenge energy from an external RF field, active tags are powered by an internal battery. In the design of temperature-sensing RFID tag, the power and energy efficiency of the co-integrated temperature sensor are important parameters. In the case of a passive tag, the sensor's power consumption limits the maximum operating distance between the tag and an external reader, while in the case of an active tag, the sensor's energy consumption limits battery lifetime. In practice, this means that temperature-sensing RFID tags require sensors that dissipate only a few micro-Watts and consume only a few tens of nano-Joule per conversion [1], [2]. A further requirement is the need for low-cost calibration techniques, due to the extreme cost constraints on RFID tags.

The required accuracy of a temperature-sensing RFID tag depends on the target application, ranging from $\pm 0.1°C$ for medical applications [3], [4] to $\pm 1°C$ for food and environmental monitoring applications [5]. Due to process spread, however, such accuracies are only achievable after calibration and trimming [6]. Temperature sensors are usually calibrated by comparing their output with that of a reference sensor at a number of known temperatures. Since both sensors need to reach thermal equilibrium, such thermal calibration can take several tens of seconds, which is incompatible with the low-cost production of RFID tags. In [7], however, a voltage calibration technique, based on electrical rather than thermal measurements, was proposed for BJT-based sensors. Since electrical measurements can be performed relatively rapidly, this is a promising low-cost calibration technique, whose utility will be further explored in this work.

Various temperature-sensing elements have been used in CMOS temperature sensors. Thermistor-based sensors can be quite energy-efficient [8]–[10], but the large spread (20–30%) and non-linear temperature dependence of on-chip resistors means that they typically require multi-point thermal calibration to achieve inaccuracies below $\pm 0.5°C$ over the military temperature range ($-55°C$ to $125°C$). MOSFETs can also be used to realize low power and energy-efficient temperature sensors [2], [4], [11]. However, the spread in gate oxide thickness and channel doping means that such sensors require one or even two-point thermal calibration to achieve inaccuracies below $\pm 1°C$ over the military temperature range. BJT-based sensors are much more accurate, requiring only a one-point thermal calibration to achieve inaccuracies less than $\pm 0.2°C$ (3σ) [13]–[16]. However, they are not particularly energy efficient, typically dissipating hundreds of nano-Joules per conversion [12].

In this paper, we describe the design of a low power, energy-efficient, low-cost BJT-based temperature sensor for RFID temperature sensing. Compared to our previous work [16], the main difference is the use of a 2nd-order switched-capacitor zoom ADC, which when combined with an improved sampling scheme, results in a $25\times$ improvement in energy efficiency compared to the state-of-the-art [12]. Moreover, the sensor is designed to facilitate low-cost voltage calibration. To study the impact of lot-to-lot spread on sensor inaccuracy, measurements on samples from two different process lots are presented. Measurements on samples in both ceramic and plastic packages are also

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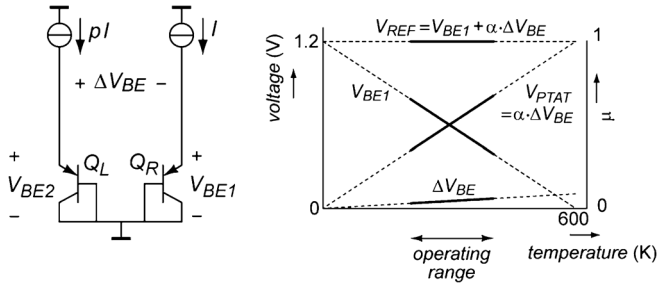

Fig. 1. Two substrate PNPs generate the required voltages (V_{PTAT} and V_{REF}) for a ratiometric temperature measurement.

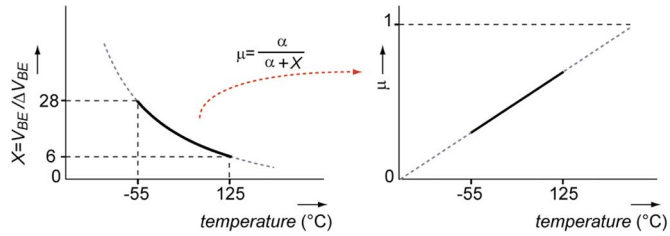

Fig. 2. Non-linear $X = V_{BE}/\Delta V_{BE}$ $(p = 5)$ and linearized $\mu = \alpha/(\alpha + X)$ as a function of temperature.

presented in order to assess the impact of the mechanical stress caused by low-cost plastic packaging. The rest of the paper is organized as follows: in the next section, the operating principle of BJT-based sensors is briefly explained and the sensor's analog front-end topology is described. Section III is devoted to the design of an energy-efficient readout circuit, while Section IV describes the implementation details. Realization and measurement results are shown in Section V, and the paper ends with conclusions.

II. Operating Principle

Fig. 1 illustrates the basic operating principle of BJT-based temperature sensors. Two identical substrate PNPs Q_R and Q_L are biased at a 1: p current ratio. The base-emitter voltage V_{BE1} of Q_R is a complementary to absolute temperature (CTAT) voltage and can be expressed as follows:

$$V_{BE1} = \eta \cdot (kT/q) \cdot ln(I_C/I_S) \tag{1}$$

where η is a process dependent non-ideality factor $(\eta \approx 1)$, k is the Boltzmann constant, q is the electron charge, T is the temperature in Kelvin, I_C is the collector current and I_S is the PNP's saturation current. In contrast to V_{BE}, the voltage difference $V_{BE2} - V_{BE1} = \Delta V_{BE}$ is proportional-to-absolute temperature (PTAT):

$$\Delta V_{BE} = V_{BE2} - V_{BE1} = \eta \cdot (kT/q) \cdot \ln(p). \tag{2}$$

Conventionally, V_{BE} (CTAT) and ΔV_{BE} (PTAT) are linearly combined to generate a band-gap reference voltage:

$$V_{REF} = V_{BE1} + \alpha \cdot \Delta V_{BE} \tag{3}$$

where α is a fixed gain factor. An analog-to-digital converter (ADC) then digitizes the ratio between $\alpha \cdot \Delta V_{BE}$ (PTAT) and the reference voltage V_{REF}. The digital ratio μ is a linear function of temperature and is given by:

$$\mu = \alpha \cdot \Delta V_{BE}/(V_{BE} + \alpha \cdot \Delta V_{BE}). \tag{4}$$

This can then be linearly scaled to obtain a digital output D_{out} in degrees Celsius:

$$D_{out} = A \cdot \mu - B \tag{5}$$

where A and B are constant coefficients: $A \approx 600$ and $B \approx 273$ [13].

A key observation is that V_{BE} and ΔV_{BE} contain all the necessary temperature information. Therefore, spending circuit resources to generate an accurate band-gap reference voltage is actually not necessary. Instead, the ratio of V_{BE} and ΔV_{BE} can simply be used as a measure of temperature [16]–[18]. As shown in Fig. 2 (left), for $p = 5$ the ratio $X = V_{BE}/\Delta V_{BE}$ is a monotonic, but non-linear function of temperature, which ranges between 6 and 28 from -55°C to 125°C. Moreover, by rewriting (4), it can be shown that the PTAT function μ can then be expressed in terms of X as follows:

$$\mu = \alpha \cdot \Delta V_{BE}/(V_{BE} + \alpha \cdot \Delta V_{BE}) = \alpha/(\alpha + X) \tag{6}$$

This calculation can be easily implemented in the digital backend. Since α is a constant in the digital domain, it is immune to process spread. As shown in Fig. 2, the constant α may be seen as a mapping coefficient between the non-linear X and PTAT μ, which can even be made variable for trimming purposes [16].

In order to minimize the sensor's energy consumption, a fast, low-power ADC is required. This is no trivial matter, since it must also achieve high resolution and accuracy [13]–[15]. Examination of Fig. 1 shows that the choice of a band-gap voltage as the ADC's reference and $\alpha \cdot \Delta V_{BE}$ as its input signal fundamentally leads to a full-scale range of about 600°C. With this approach, state-of-the-art accuracy has been achieved over the military temperature range [13]. So in-line with the sensor's expected 0.2°C inaccuracy [16], the ADC must achieve 12-bit accuracy and even better resolution to facilitate calibration and trimming. In the following, an ADC architecture is presented that meets these requirements, while also meeting the power and energy constraints of RFID tags.

III. Zoom-ADC

In most cases, temperature changes are rather slow, and so X can be digitized by a two-step or zoom ADC that employs a coarse SAR phase and a fine $\Delta\Sigma$-ADC phase [16]. As shown in Fig. 3(a), the ratio X ranges from 6 to 28 $(p = 5)$ over the military temperature range. It can thus be expressed as $X = n + \mu'$, where n and μ' are its integer and fractional parts, respectively. The integer n can then be determined in five successive approximation steps, (Fig. 3(a)). During the succeeding fine conversion, the references of a $\Delta\Sigma$-ADC are chosen so as to zoom

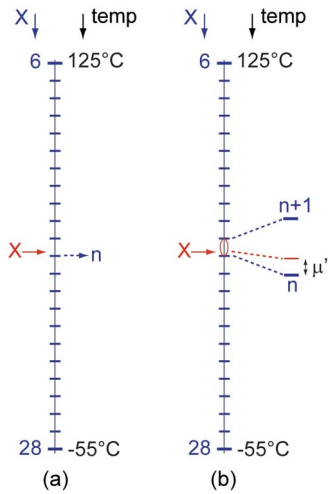

Fig. 3. Temperature dependence of $X = n + \mu'$ from $-55°$C to 125°C. The integer n ranges between 6 and 28 (a) while the fraction μ' ranges between 0 and 1 (b).

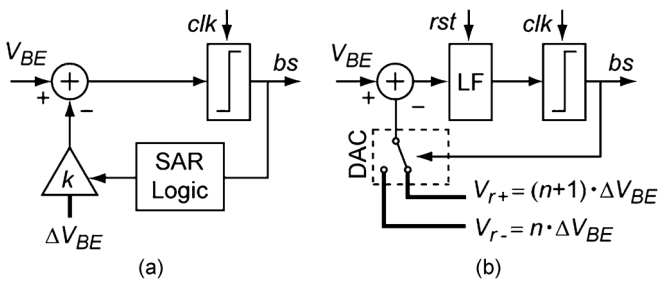

Fig. 4. Block diagram of the zoom ADC during the coarse (a) and fine (b) conversions.

into the range between n and $(n+1)$, whereupon the fraction μ' can be determined with higher resolution (Fig. 3(b)). Due to this zoom-in phase, the resolution requirements on the $\Delta\Sigma$-ADC are greatly relaxed, leading to simple, low power analog circuitry.

Fig. 4 illustrates the operation of a zoom ADC during the coarse and fine phases. During the coarse conversion phase, a clocked comparator compares V_{BE} to integer multiples of ΔV_{BE} (Fig. 4(a)). In five steps, the SAR logic in the feedback loop adjusts the gain factor k until the integer n is found. The references of a $\Delta\Sigma$-ADC are then set to $n \cdot \Delta V_{BE}$ and $(n+1) \cdot \Delta V_{BE}$ as shown in Fig. 4(b). Since the net integrated charge is forced to be approximately zero by the feedback loop, the bitstream average is the desired $\mu' = (V_{BE} - n \cdot \Delta V_{BE})/\Delta V_{BE}$.

In practice, the range in the fine conversion step is doubled so that the input X is always roughly in the middle of the extended range. This accomodates small errors during the coarse phase and also ensures that X lies within the useable range of the $\Delta\Sigma$ modulator. The necessary information is obtained during a guard-band step, in which V_{BE} is compared to $(n+0.5)\cdot\Delta V_{BE}$ [17]. Depending on the result, the references of the $\Delta\Sigma$-ADC are then set to either $(n-1)\cdot\Delta V_{BE}$ and $(n+1)\cdot\Delta V_{BE}$, or $n \cdot \Delta V_{BE}$ and $(n+2)\cdot\Delta V_{BE}$. In the rest of the paper, for simplicity, we shall assume that the former is the case.

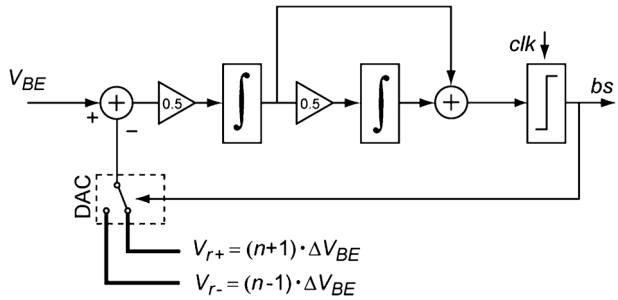

Fig. 5. Block diagram of the proposed 2nd-order zoom ADC during the fine conversion.

A. Improving Conversion Speed

In previous work, a zoom-ADC based on a 1st-order $\Delta\Sigma$-ADC was used in a low power temperature sensor [16]. Its energy-efficiency, however, was limited by the inherently low conversion rate of its 1st-order modulator. Furthermore, to achieve the required 13-bit resolution, an opamp with a DC gain in excess of 80 dB was necessary, which in the target 0.16 μm CMOS process led to a topology with limited power efficiency.

In this work we propose a 2nd-order zoom ADC, which is about 8$\times$ faster and requires integrators with lower gain than its 1st-order counterpart, thus leading to significantly improved power and energy efficiency. As shown in Fig. 5, it is based on a single-bit feed-forward 2nd-order $\Delta\Sigma$-ADC. Since $V_{BE} \sim n \cdot \Delta V_{BE}$ during the fine conversion step, the error signal processed by the loop filter is quite small, thus reducing the output swing of the two opamps. As a result, no extra feed-forward path between the input terminal and the quantizer's input is required, as is the case in the well-known low-swing feed-forward architecture [19]. This simplifies the modulator's implementation, reduces the loading on the analog front-end that generates V_{BE}, and eliminates a potential source of parasitic coupling into the summing node at the quantizer's input.

B. An Energy-Efficient Integration Scheme

During the fine conversion, as shown in Fig. 5, every $\Delta\Sigma$ cycle requires the integration of either $(V_{BE} - (n-1)\cdot\Delta V_{BE})$ or $(V_{BE} - (n+1)\cdot\Delta V_{BE})$, when the comparator's output bs is either 0 or 1, respectively. For simplicity, let's assume that a charge proportional to $(V_{BE} - k\cdot\Delta V_{BE})$ is integrated during one $\Delta\Sigma$ cycle, where k is either $(n-1)$ or $(n+1)$ depending on the polarity of bs. In [16], this was performed in two clock cycles by a SC integrator. In a first clock cycle a charge proportional to V_{BE} was integrated, while in a second clock cycle a charge proportional to $-k\cdot\Delta V_{BE}$ was integrated.

In this work, the two clock cycles are combined i.e. both V_{BE} and ΔV_{BE} are simultaneously sampled and then integrated in *one* clock cycle. As shown in Fig. 6, during the sampling phase ϕ_1, V_{BE} is sampled on C_S while $-\Delta V_{BE}$ is simultaneously sampled on $k\cdot C_S$, thus a charge proportional to $(V_{BE} - k\cdot\Delta V_{BE})$ is stored on the sampling capacitors. The polarity of both input voltages is swapped during ϕ_2, and therefore a charge proportional to $2\cdot(V_{BE} - k\cdot\Delta V_{BE})$ is integrated during *each* clock cycle. Due to the charge cancellation between V_{BE} and

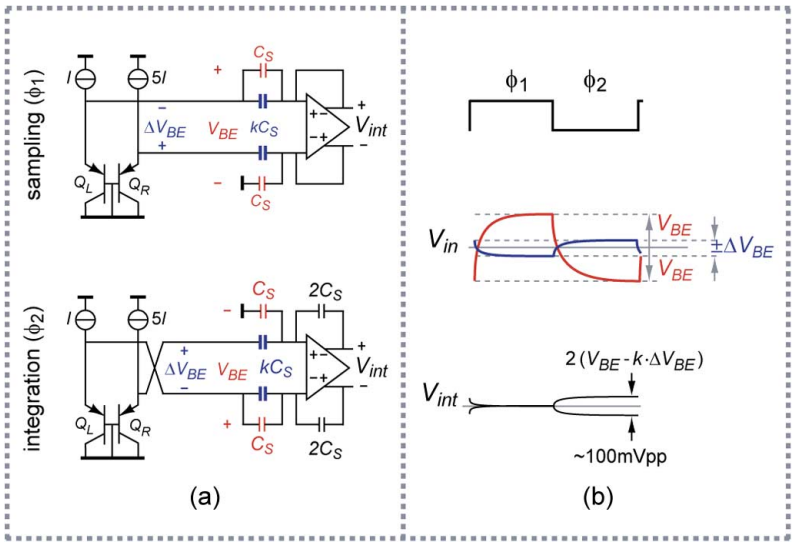

Fig. 6. (a) Proposed integration scheme during sampling (ϕ_1) and integration (ϕ_2) phases. (b) Waveforms of a full SAR/$\Delta\Sigma$ cycle. V_{in}: zoom ADC's input voltage, V_{int}: integrator's output voltage. Parameter k is set by the SAR logic in the coarse conversion, while $k = n - 1$ or $n + 1$ when $bs = 0$ or 1 in the fine conversion step.

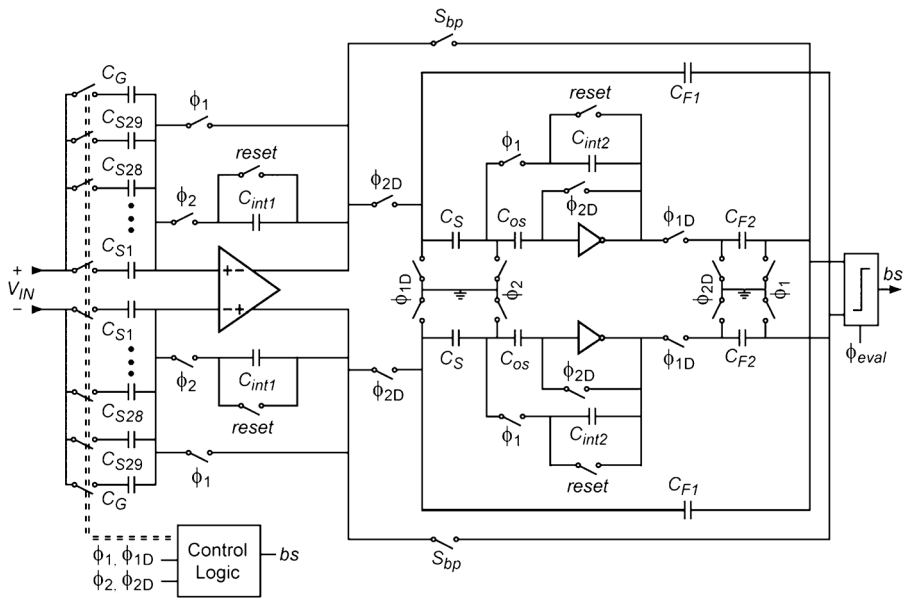

Fig. 7. Simplified circuit diagram of the proposed 2nd-order zoom ADC.

$-k \cdot \Delta V_{BE}$, the integrated charge difference is quite small, and can be accommodated by a low-swing, and power-efficient telescopic opamp. This is in contrast with [16], where a folded-cascode opamp was required. Moreover, this approach also halves the conversion time, thus improving the energy efficiency by another factor of two.

IV. Implementation

A. Circuit Diagrams

Fig. 7 shows the simplified circuit level diagram of the proposed 2nd-order zoom ADC. A capacitor DAC with 28, 120 fF unit capacitances realizes the gain factor k required for ΔV_{BE} amplification, while an extra capacitor $C_G = 0.5 \cdot C_S$ is used during the guard-band step. To simultaneously sample V_{BE}, the number of unit elements in the capacitor DAC is increased to 29. During the coarse conversion step, a switch S_{bp} bypasses the 2nd integrator, thus directly connecting the output of the first integrator to the comparator. Moreover, at the start of each comparison step, the first integrator is reset, and therefore it acts as a sample-and-hold.

The first integrator is built around a power-efficient, fully differential telescopic opamp, which draws 600 nA, has a gain of 76 dB, and a maximum swing of about ±200 mV. As shown in Fig. 7, a pseudo-differential inverter-based OTA forms the second integrator [20]. At 25°C, it draws 140 nA, occupies only 0.002 mm^2, and has a gain of ∼44 dB. During ϕ_2, when the output of 1st integrator is sampled on capacitors C_S, the two inverter-based OTAs are in unity-gain configuration and auto-zeroed via offset storing capacitors C_{OS}. Due

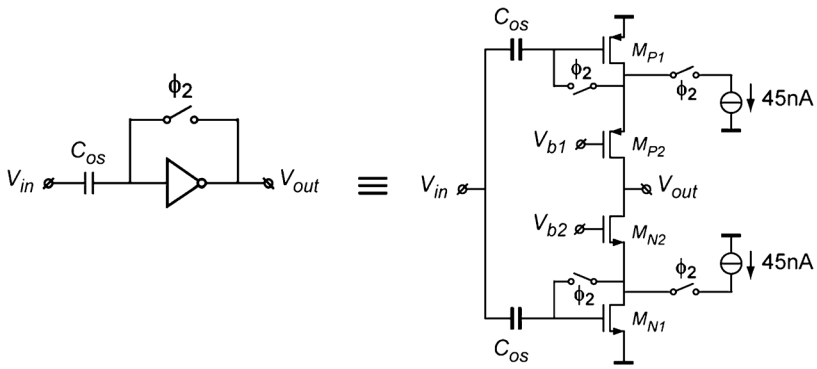

Fig. 8. Circuit diagram of the proposed inverter-based OTA.

to the feedback path through the integration capacitors in ϕ_1, a virtual ground is formed, thus pushing the sampled charge into the integration capacitors $C_{int2} = 2 \cdot C_S$. Fig. 8 shows the implementation details of one of the inverter-based OTAs. To decrease the inverter's sensitivity to power supply and process spread, a dynamic current-biasing technique is proposed. During the auto-zeroing phase ϕ_2, M_{N1} and M_{P1} are diode-connected and biased with two current sources (45 nA each), while their operating bias voltages are stored on offset storing capacitors C_{OS}. The bias voltages $\mathrm{V_{b1}}$ and $\mathrm{V_{b2}}$ are chosen such that $\mathrm{M_{N2}}, \mathrm{M_{P2}}$ are essentially "off" during ϕ_2. The two currents are mirrored from the front-end's precision bias circuit to ensure robustness to supply and process variations. After disconnecting the two current sources in ϕ_1, M_{N1} and M_{P1} are configured as common-source and form a class-AB amplifier, with a virtual ground at V_{in}. Since the output voltage swing requirement is reduced to about ± 100 mV by the prior coarse conversion step, cascoding of M_{N1} and M_{P1} is readily possible, thus enhancing the inverter's output resistance, and hence its DC gain. A passive summation network at the input of quantizer combines the output of 2nd integrator with that of the 1st integrator via the feed-forward capacitor C_{F1}, as shown in Fig. 7. To set-up the various biasing voltages, the ADC requires a startup time of 120 μsec (3 clock cycles) before each conversion.

B. Precision Techniques

During the fine conversion, the accuracy of the ratio k is determined by the matching between the unit capacitor that samples V_{BE} and the k capacitors which sample ΔV_{BE}. Any mismatch will lead to a non-linear ADC transfer function. The matching of the references should, therefore, be commensurate with the ADC's target resolution, i.e. 13-bit. Since this cannot be achieved by layout alone, a dynamic element matching (DEM) scheme was used.

Fig. 9 shows the block diagram of the sensor and the timing of a full temperature conversion. The analog front-end consists of a bias circuit and a bipolar core. The bias circuit generates a PTAT current $I = 90$ nA (at 25°C) with the help of a low power, self-biased chopped opamp and two auxiliary PNPs [16]. Since the transistor's current gain β_F ($\sim$5 in the process used) will be impacted by process spread, a β_F-compensation technique is employed to ensure that Q_R and Q_L are biased with β_F-independent *collector* currents, thus improving the robustness of the resulting V_{BE} to process spread. This only requires the addition of a resistor $R_b/5$ in series with the base of Q_{BL} [13]. Furthermore, the six current sources and the two bipolar transistors in the bipolar core are dynamically matched to achieve (on average) the accurate 1:5 current ratio required to generate an accurate ΔV_{BE} [13].

A major source of inaccuracy, the offset and $1/f$ noise of integrators, is reduced by employing corrolated-double sampling (CDS) during the coarse and fine conversions [13]. In order to minimize the effect of charge injection, both integrators use differential topologies with minimum-size switches around the integration capacitors. In contrast to [16], a digital rather the conventional analog implementation of system-level chopping is employed, in order to further lower the modulator's residual offset. As shown in Fig. 9, after an initial coarse conversion, the $\Delta\Sigma$ conversion is performed twice with swapped input voltage polarities, and the two digital results are then averaged [20]. This eliminates the need for state-preserving choppers around the integration capacitors [13], [16] which simplifies the layout and eliminates a potential source of charge injection, which could otherwise cause ADC non-linearity. Compared to the conventional analog approach, however, this results in a small loss in resolution: up to 0.5 bits if the ADC is quantization-noise limited.

V. Realization and Measurements

The sensor was realized in a standard 0.16 μm CMOS process with five metal layers, and has an active area of 0.08 mm^2, as shown in Fig. 10. For flexibility, the digital back-end, the control logic and the fine conversion's sinc^2 decimation filter [21] were implemented off-chip. At 25°C, the sensor draws 3.4 μA and operates from a 1.5 V to 2 V supply with a supply sensitivity of 0.5°C/V. Running at a clock frequency of 25 kHz, it requires a conversion time of 5.3 msec (128 $\Delta\Sigma$ cycles) to achieve a kT/C limited resolution of 20 mK (rms), which improves to about 5 mK (rms) if the conversion time is extended to 100 msec. For characterization, 18 devices from one batch were packaged in ceramic DIL packages and measured over the military temperature range from -55°C to 125°C. As shown in Fig. 11 the resulting inaccuracy after batch calibration was ± 0.6°C (3σ), with a residual curvature of only ± 0.03°C. To further improve the sensor's accuracy, individual calibration and trimming is essential. In the following, two different approaches based on thermal and electrical measurements are presented.

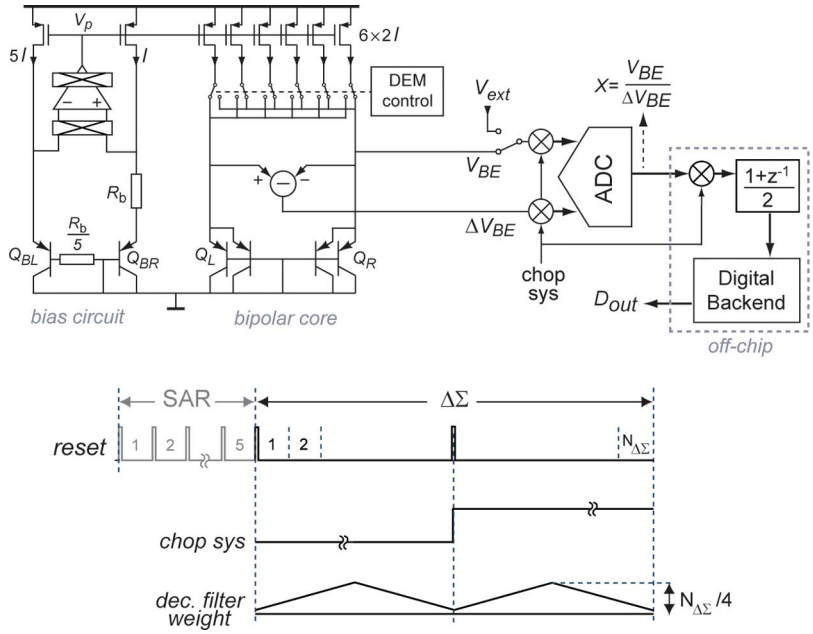

Fig. 9. Top: Block diagram of the temperature sensor. Bottom: timing diagram of a full temperature conversion.

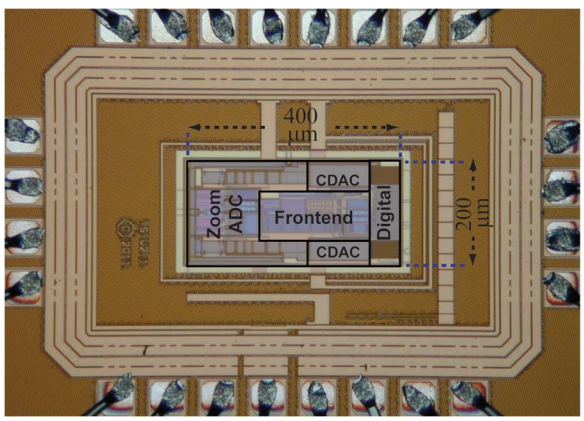

Fig. 10. Chip micrograph of the sensor.

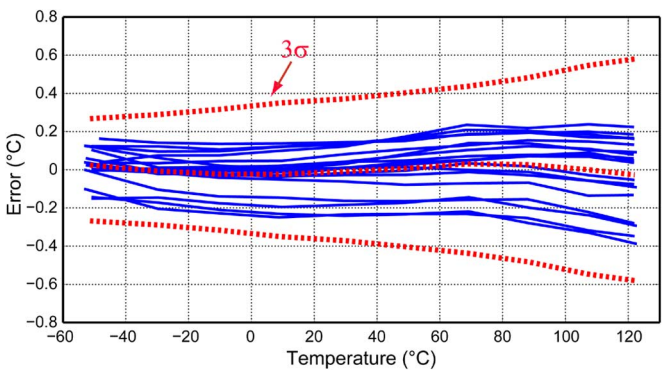

Fig. 11. Measured temperature error of 18 sensors before trimming; dashed lines refer to the average and $\pm 3\sigma$ limits.

A. Thermal Calibration

Individual calibration of an integrated temperature sensor requires accurate information about its die temperature. Conventionally, this is obtained by bringing the device under test (DUT) and a reference temperature sensor to exactly the same temperature, whereupon the outputs of both devices are logged. In this work, the reference sensor is a platinum Pt-100 resistor calibrated to an inaccuracy of 20 mK. Both sensors are embedded in a large metal block, which acts as a thermal low-pass filter and facilitates measurements with milli-Kelvin stability [22].

Three different single-parameter trimming methods were investigated. First, for each sensor, the offset parameter B in (5) was adjusted so as to cancel the error at the calibration temperature (30°C). After this offset trim, the sensor's inaccuracy is less than $\pm 0.25^{\circ}$C (3σ) from -55°C to 125°C. Alternatively, the parameter α in (6) can be adjusted, as in [16], [17]. The resulting inaccuracy, however, is almost exactly the same as that obtained with offset trim. Since the dominant source of sensor inaccuracy, i.e. the spread in V_{BE}, is PTAT in nature (see Fig. 11), a digital PTAT trim can also be employed [23]. This is carried out in the digital backend by modifying (5) as follows:

$$D_{out} = A \cdot \frac{\mu}{1 - \gamma_D \mu} - B \tag{7}$$

Here γ_{D} is a calibration constant that is determined as follows:

$$\gamma_D = \frac{1}{\mu} - \frac{1}{\mu_{ideal}} \tag{8}$$

where μ_{ideal} is the desired ratio at the calibration temperature. The resulting inaccuracy is then less than $\pm 0.15^{\circ}$C (3σ), as shown in Fig. 12.

B. Voltage Calibration

Although thermal calibration can be performed very accurately, the long stabilization time required for the DUT and the reference sensor to reach thermal equilibrium prohibits its use as a low-cost calibration method. In [7], a voltage calibration method was proposed, in which die temperature is established by measuring an on-chip ΔV_{BE}. By applying DEM to

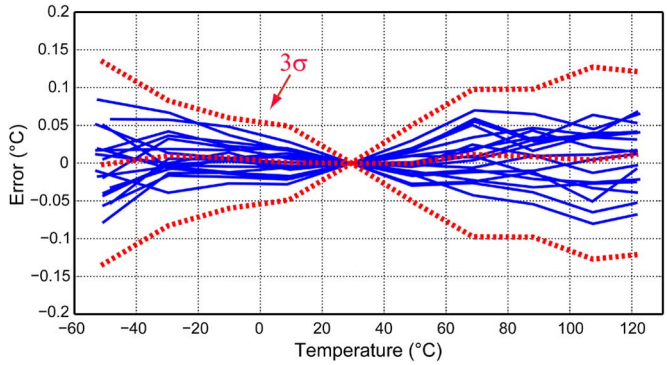

Fig. 12. Measured temperature error of 18 sensors after thermal calibration and PTAT trimming at 30°C; dashed lines refer to the average and $\pm 3\sigma$ limits.

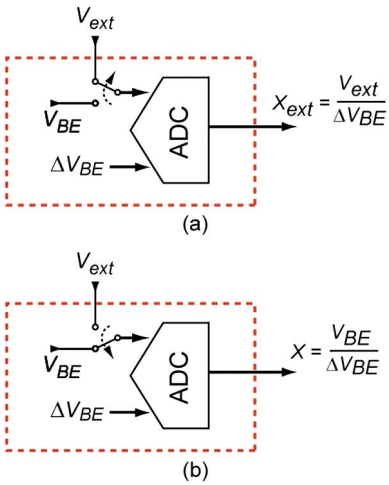

Fig. 13. Voltage calibration requires only two ADC conversions: first the actual die temperature is obtained (a) and then a normal conversion gives the untrimmed output (b).

the six current sources and the two PNPs (see Fig. 9), the collector current ratio p, and therefore ΔV_{BE} can be made robust to process spread. The process-dependent non-ideality factor $\eta(=\ 1.0042)$ can also be extracted by batch calibration. As shown in Fig. 13, the die temperature can then be determined by the following procedure. First, V_{BE} is replaced by an accurate external voltage V_{ext} (see Fig. 13(a)). The on-chip ADC then digitizes the ratio $X_{ext} = V_{ext}/\Delta V_{BE}$ accurately and with high resolution, whereupon the actual die temperature T_D can be calculated:

$$\Delta V_{BE} = \eta \cdot \frac{kT_D}{q} \cdot \ln(p), \qquad X_{ext} = \frac{V_{ext}}{\Delta V_{BE}}$$
$$\Rightarrow T_D = \frac{V_{ext}}{C_m \cdot X_{ext}}, \qquad C_m = \eta \cdot \frac{k}{q} \cdot \ln(p) \qquad (9)$$

In a second step, V_{ext} is replaced by the on-chip V_{BE} and a normal conversion is performed to determine $X = V_{BE}/\Delta V_{BE}$, and hence the sensor's untrimmed output (see Fig. 13(b)). In contrast to thermal calibration, this approach can be performed at room temperature, and is much faster, requiring only two ADC conversions. Since the sensor achieves a resolution of 5 mK in a conversion time of 100 msec, which is commensurate with the expected ± 0.15°C inaccuracy, this means that the total calibration time is only 200 msec.

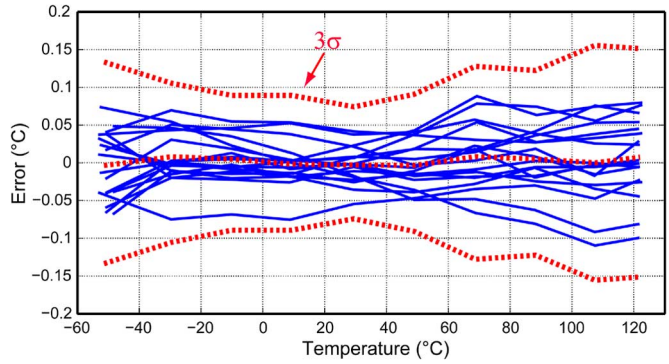

Fig. 14. Measured temperature error of 18 sensors after voltage calibration and PTAT trimming at room temperature; dashed lines refer to the average and $\pm 3\sigma$ limits.

TABLE I
IMPACT OF LOT-TO-LOT SPREAD ON SENSOR ACCURACY AND CALIBRATION PARAMETERS

	Lot-1	Lot-2
Untrimmed inaccuracy (3σ)	±0.6°C	±0.6°C
PTAT-trimmed inaccuracy (3σ)	±0.15°C	±0.25°C
α (mapping coefficient)	15.44	15.45
A (gain parameter)	613.31	610.74
B (offset parameter)	283.70	282.93
η (non-ideality factor)	1.0042	1.0044

TABLE II
EFFECT OF MECHANICAL STRESS ON SENSOR ACCURACY AND CALIBRATION PARAMETERS

	Ceramic Package	Plastic Package
Untrimmed inaccuracy (3σ)	±0.6°C	±0.8°C
PTAT-trimmed inaccuracy (3σ)	±0.25°C	±0.25°C
α (mapping coefficient)	15.45	15.47
A (gain parameter)	610.74	611.59
B (offset parameter)	282.93	283.94
η (non-ideality factor)	1.0044	1.0044

Compared to the results of thermal calibration, the results of voltage calibration followed by an offset or digital PTAT trim are only slightly worse around room temperature. The worst-case inaccuracy from -55°C to 125°C, however, is almost exactly the same as shown in Fig. 14. This confirms the fact that the inaccuracy of ΔV_{BE} is negligible, and so voltage calibration is a robust alternative to thermal calibration.

C. Lot-to-Lot Spread

To verify the effect of lot-to-lot spread on sensor inaccuracy, devices from a different process lot were characterized. As before, 18 devices from one batch were packaged in ceramic DIL packages and measured from -55°C to 125°C. Table I compares the resulting inaccuracy and calibration parameters (i.e. A, B, and α) of the two lots. As shown, the resulting inaccuracy after PTAT trimming has increased to ± 0.25°C (3σ). Moreover, the obtained gain and offset parameters A, B after batch calibration show a lot-to-lot spread of about 0.4% and 0.3%, re-

TABLE III
PERFORMANCE SUMMARY AND COMPARISON TO PREVIOUS WORK

Parameter	**This work**	[16]	[9]	[11]
Sensor type	**BJT**	BJT	Resistor	MOSFET
CMOS Technology	**0.16μm**	0.16μm	0.18μm	0.18μm
Chip area	**0.08mm^2**	0.12mm^2	0.18mm^2	0.032mm^2
Supply current †	**3.4μA**	4.6μA	20μA	0.4μA
Supply voltage	**1.5V to 2V**	1.6V to 2V	1.2-2.0V	0.9-1.1V
Supply sensitivity	**0.5°C/V**	0.1°C/V	0.625°C/V	8°C/V
Inaccuracy	**±0.15°C (3σ)**	±0.2°C (3σ)	±0.5°C (max)	−0.8/+1°C (max)
Temperature range	**–55°C to 125°C**	–30°C to 125°C	0°C to 100°C	0°C to 100°C
Calibration (points)	**voltage (1)**	thermal (1)	thermal (1)	thermal (2)
Resolution (T_{conv})	**0.02°C (5.3ms) 0.005°C (100ms)**	0.015°C (100ms)	0.25°C (12.5μs)	0.3°C (1ms)
Resolution FoM †	**11pJ°C^2**	170pJ°C^2	19pJ°C^2	32pJ°C^2
Accuracy FoM †	**0.75nJ%^{2}**	49nJ%^{2}	0.3nJ%^{2}	1.17nJ%^{2}

Res. FoM = Energy/Conversion × (Resolution)^2, Acc. FoM = Energy/Conversion×(Relative inaccuracy)^2
Relative inaccuracy(%) =100 × Max Error/Specified temperature range
† Excluding the off-chip digital

spectively. Since at room temperature the PTAT ratio $\mu \approx 0.5$, this translates to a temperature shift of about -0.5°C, from (5). However, the optimal mapping coefficient α changes by less than 0.1% from lot-to-lot. This small variation can be readily compensated by modifying the calibration parameters (A and B) without sacrificing accuracy, and so α can be regarded as a digital constant. Finally, the non-ideality factor η only changes by about 0.02% from lot-to-lot, which corresponds to a maximum calibration error of about 50 mK.

D. Plastic Packaging

In production, low-cost plastic packages are preferred to ceramic packages. The associated mechanical stress, however, impacts the sensor's accuracy, an effect which is referred to as packaging shift [24], and results in a fairly systematic modification to the base-emitter voltage V_{BE} [25], [26]. To evaluate this, 22 samples from the same batch of the second lot were packaged in plastic DIP packages and then characterized. As shown in Table II, the untrimmed inaccuracy after batch calibration increased to about $\pm 0.8^\circ$C (3σ). However, a PTAT trim reduced the inaccuracy to about $\pm 0.25^\circ$C (3σ), which is equivalent to that obtained with ceramic packaging. The optimal mapping coefficient α changed by about 0.2%, while the fitting parameters A, B changed by about 0.15% and 0.35% respectively, which corresponds to a packaging shift of about -0.36°C at room temperature.

From these measurements, it can be concluded that batch calibration is essential to achieving high accuracy over different lots and different packages. Once the fitting parameters A and B are known, individual devices can be trimmed on the basis of a fast voltage calibration, since the non-ideality parameter is essentially constant over different lots and packages.

E. Noise and ADC Characteristic

As in other two-step ADC structures, mismatch between the references used in the various fine conversion steps could result in discontinuities in the ADC's characteristic. To examine this, the ADC's input range was swept by slowly sweeping the oven temperature from -40°C to 100°C over a three hour period, while continuously logging the sensor's output. This corresponds to a temperature slope of ≈13 mK/sec, which implies that the temperature change between successive measurements is less than 1 mK, much smaller than the sensor's own resolution. Taking the difference between successive sensor outputs then results in a pseudo-DNL function, which reflects the ADC's resolution and possible discontinuities between the various fine conversion segments. As shown in Fig. 15, the sensor achieves a resolution of 20 mK (rms) into 5.3 ms around room temperature ($X \approx 14.5$), which is enough to calibrate it rapidly to 0.2°C inaccuracy. Moreover, there are no discontinuities between the different fine segments. Lastly, it can be seen that the sensor's resolution is slightly temperature dependent. This is due to the fact that the full-scale range of each fine conversion is not constant, but is equal to $2 \cdot \Delta V_{BE}$.

F. Comparison to Previous Work

The sensor's performance is summarized in Table I and compared to other energy-efficient, low power state-of-the-art temperature sensors. It is the only sensor which employs a low-cost, room-temperature voltage calibration technique, and

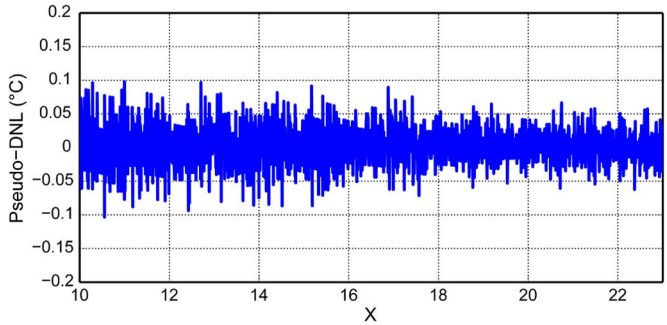

Fig. 15. Measured Pseudo-DNL versus X. The sensor's conversion time is 5.3 msec.

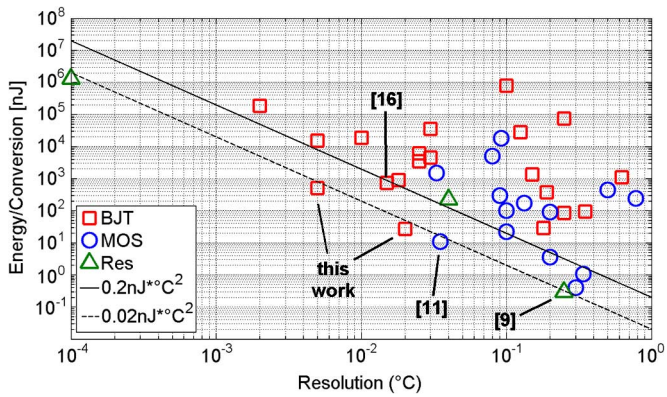

Fig. 16. Energy per conversion versus resolution for different smart temperature sensors using different sensing principles [12].

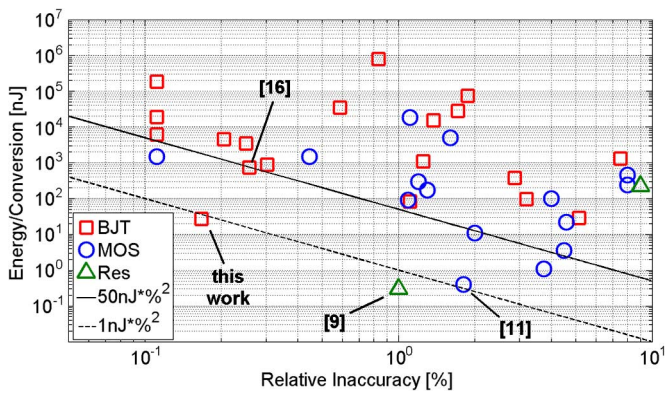

Fig. 17. Energy per conversion versus relative inaccuracy for different smart temperature sensors using different sensing principles [12].

it also achieves the highest accuracy: $\pm 0.15°\text{C}$ (3σ) from $-55°\text{C}$ to $125°\text{C}$. Compared to the other BJT-based sensor, this work achieves comparable resolution in about $18\times$ less conversion time, while consuming 25% less supply current. Fig. 16 compares the sensor's performance in terms of energy/conversion and resolution with several other smart temperature sensors [12]. For two different resolutions and conversion rates ($0.02°\text{C}$ @ 5.3 msec and $0.005°\text{C}$ @ 100 msec), the sensor achieves nearly the same resolution FoM: 11 pJ°C^2. In Fig. 17, the energy/conversion versus relative inaccuracy for the same set of sensors is also shown [12]. It can be seen that this work achieves an accuracy FoM of 0.75 nJ$\%^2$. For the specific class of BJT-based temperature sensors, this represents over $15\times$ improvement and is in line with the performance of state-of-the-art thermistor- and MOSFET-based sensors.

VI. Conclusions

A BJT-based smart temperature sensor for RFID applications has been implemented in a 0.16 μm CMOS technology. To meet the extreme low-power, low-energy requirements on RFID tags a 2nd-order zoom ADC has been developed. It combines the benefits of SAR-and 2nd-order $\Delta\Sigma$-ADCs to perform accurate, high resolution readout of the voltages on two sensing BJTs while minimizing power and energy consumption. Moreover, a new charge-balancing scheme is proposed, which reduces ADC conversion time by another factor $2\times$ and allows the use of low-swing, and therefore low-power opamps, thus further improving the sensor's energy efficiency. After an accurate thermal calibration at 30°C and a PTAT trim the sensor achieves an inaccuracy of $\pm 0.15°\text{C}$ (3σ) from $-55°\text{C}$ to $125°\text{C}$. To meet the extreme cost constraints on RFID tags, a voltage calibration technique based on electrical measurements was also explored. Compared to thermal calibration, it is significantly faster, requiring only two ADC conversions (200 msec), while achieving comparable accuracy.

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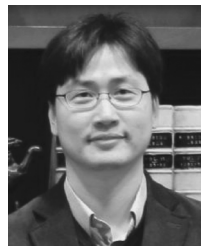

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