12.7 A 0.85V 600nW All-CMOS Temperature Sensor with an Inaccuracy of ±0.4°C (3σ) from -40 to 125°C

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This paper describes an all-CMOS temperature sensor intended for RFID applications that achieves both sub-1V operation and high accuracy (±0.4°C) over a wide temperature range (-40 to 125°C). It is also an ultra-low-power design: drawing 700nA from a 0.85V supply. This is achieved by the use of dynamic threshold MOSTs (DTMOSTs) as temperature-sensing devices, which are then read out by an inverter-based 2nd-order zoom ADC. Circuit errors are mitigated by the use of dynamic error-correction techniques, while DTMOST spread is reduced by a single room temperature (RT) trim. The latter feature constitutes a significant advance over previous all-CMOS designs [5,6], which require two-point trimming to approach the same level of accuracy.

In most CMOS processes, a diode-connected DTMOST can be readily realized by connecting the gate, bulk and drain of a standard PMOST together (Fig. 12.7.1). The resulting device approximates an ideal diode, with an extrapolated gate-source voltage V_{GS}~ 0.6V at 0K and a linear temperature coefficient of about -1mV/°C [2]. Connecting the gate to the bulk reduces the influence of gate-oxide thickness on the resulting dynamic threshold voltage, and thus the V_{GS} spread of a DTMOST is significantly less than that of a normal PMOST [1,2]. Diode-connected DTMOSTs can thus be used to replace the BJTs of a conventional band-gap voltage reference [2] or temperature sensor [1]. However, since the magnitude of V_{GS} (~ 0.3V at RT) is only about half that of a BJT's base-emitter voltage V_{BE} (~ 0.6V at RT), the resulting circuit can be operated at supply voltages below 1V over a wide temperature range, e.g., from -40 to 125°C.

The sensor's front-end is shown in Fig. 12.7.1. A pair of DTMOSTs with a 1:2 area ratio that are biased by identical currents I=90nA (at RT). The same currents also power a so-called current-voltage mirror (CVM) [3], which forces a proportional-to-absolute-temperature (PTAT) voltage ΔV_{GS} across a resistor. As a result, the biasing currents will also have a well-defined PTAT dependency. To minimize the effect of DTMOST mismatch, which would otherwise impact the accuracy of ΔV_{GS}, the 1:2 area ratio is established by incorporating three unit DTMOSTs into a dynamic element matching (DEM) scheme. Since the associated DEM switches carry bias current, Kelvin connections are used to accurately read out V_{GS} and ΔV_{GS}. Another source of error is the CVM's offset and 1/f noise, which add directly to ΔV_{GS} and thus impact the accuracy of the bias currents, and hence of both V_{GS} and ΔV_{GS}. Such errors are mitigated by chopping the CVM (Fig. 12.7.1).

The sensor's block diagram is shown in Fig. 12.7.2. It consists of the DTMOST front-end, a 2nd-order incremental zoom ADC, a voltage doubler and some control logic. As in [4], the zoom ADC uses a power-efficient coarse/fine algorithm to convert the front-end's output voltages V_{GS} and ΔV_{GS} into a temperature-dependent ratio $X = V_{GS}/\Delta V_{GS}$. In this design, X varies from 5 to 28 over the temperature range –40 to 125°C. An off-chip digital backend then computes a PTAT function of temperature $\mu = \alpha/(\alpha+X)$, where α is a gain factor, which can be trimmed to compensate for V_{GS} spread. The sensor has two supply voltages: an analog supply AVDD, which powers the front-end and the ADC, and a digital supply DVDD, which powers the voltage doubler. The output of the doubler drives the logic that, in turn, drives the switches that sample V_{GS} and ΔV_{GS}, thus facilitating the use of sub-1V supply voltages. To minimize its residual offset, the entire ADC is chopped over two conversions.

As shown in Fig. 12.7.2, the zoom ADC digitizes the output of the DTMOST front-end in a two-step manner [4]. Each zoom ADC conversion begins with a coarse SAR conversion followed by a fine ΔΣ conversion to generate the ratio $X = V_{GS}/\Delta V_{GS}$. The coarse conversion determines the integer part of X, or n, by using a 5b SAR algorithm to compare V_{GS} with integer multiples of ΔV_{GS} (Fig. 12.7.2). The fractional part of X, or μ', is then determined by a 2nd-order incremental ΔΣ-ADC, whose reference voltages are arranged to straddle V_{GS} by setting them to $n{\cdot}\Delta V_{GS}$ and $(n{+}2){\cdot}\Delta V_{GS}$. The resulting $2\Delta V_{GS}$ input range provides redundancy, thus relaxing the requirements on the coarse conversion, and ensuring that the modulator is not overloaded.

The heart of the zoom ADC is a feed-forward 2nd-order SC ΔΣ-ADC (Fig. 12.7.3). At its input is a capacitive-DAC (cap-DAC) with 30 unit elements (each 60fF), which can sample either V_{GS} or $k{\cdot}\Delta V_{GS}$, where k = 1..30. In contrast to [4], both integrators are formed around pseudo-differential inverter-based amplifiers, thus fully exploiting the reduced integrator swing conferred by zooming. The first integrator draws 135nA while the, less critical, 2nd integrator draws only 66nA. These current levels are defined with the help of a dynamic biasing technique that simultaneously auto-zeros each amplifier [4]. During the coarse conversion, the first integrator computes V_{GS} - $k{\cdot}\Delta V_{GS}$, while its output is connected directly to the comparator via the switch S_{bp}. Off-chip logic then implements the SAR algorithm by applying trial values k to the chip and monitoring the comparator's output.

During the fine conversion, the mismatch between the unit elements of the cap-DAC is mitigated by the use of DEM. In contrast to [4], the required DEM logic is implemented on-chip (Fig. 12.7.4). It consists of a 30b circular shift-register (SR), with an effective length (defined by a periodic reset signal) of n+3 bits, where n is the result of the coarse conversion. Resetting the SR loads it with a single logic "1," which then circulates on every succeeding clock pulse. This bit (via the m_i outputs) is used to select the capacitor that samples V_{GS}, while the other bits define the n+2 capacitors that *may* be used to sample ΔV_{GS}. Depending on the bitstream output (bs), either n or n+2 capacitors will be selected (via the t_i outputs). The SR is reset during the coarse conversion, so that the same capacitors are always used for the SAR conversion. The DTMOST's DEM logic is implemented by a separate 3b SR.

The prototype sensor is realized in a standard 0.16µm CMOS process (Fig. 12.7.7). It occupies 0.085mm², and draws 700nA from a 0.85V supply. The front-end and ADC draw 560nA, while the voltage doubler and the rest of the on-chip digital circuitry draw 140nA. For flexibility, the SAR logic and the sinc² decimation filter are implemented off-chip. However, simulations show that implementing them on-chip would only incur an extra 10nW per conversion. With DVDD fixed at 0.9V, AVDD was varied from 0.85V to 1.2V. The corresponding supply sensitivity of the front-end and ADC was 0.45°C/V.

A total of 16 devices in ceramic DIL packages were characterized over the temperature range from –40 to 125°C. As shown in Fig. 12.7.5 (top), their batch-calibrated inaccuracy was ±1°C (3σ, 16 devices), with a residual curvature of only 0.03°C. After an alpha trim at 30°C, the inaccuracy improves to ±0.4°C (3σ), as shown in Fig. 12.7.5 (bottom). Offset trimming, as in [1], is slightly worse, resulting in an inaccuracy of ±0.5°C (3σ). These results show that DTMOSTs, like BJTs, can be effectively trimmed at a single temperature.

While running at a clock frequency of 25kHz, the sensor requires only 3.6nJ to achieve a kT/C-limited resolution of 63mK (rms) in a conversion time of 6ms. This corresponds to a resolution FoM of 14.1pJK², which is in line with the state of the art [4]. The sensor's performance is summarized in Fig. 12.7.6 and compared to that of other state-of-the-art low-voltage designs. It can be seen that, except for the BJT-based design [4], this sensor is 2-to-3× more accurate than the rest, while also achieving the best energy efficiency.

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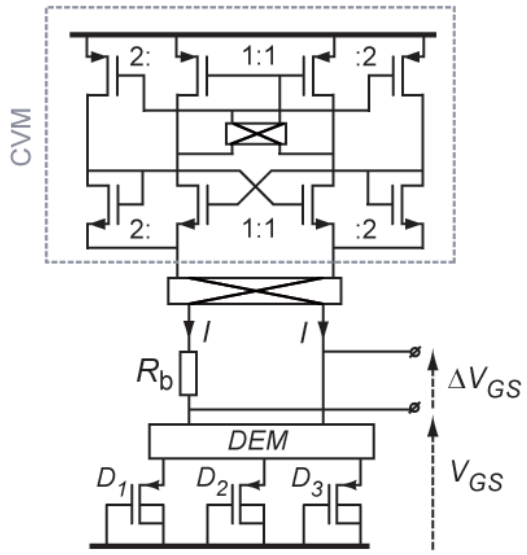

Figure 12.7.1: DTMOST-based sensor front-end.

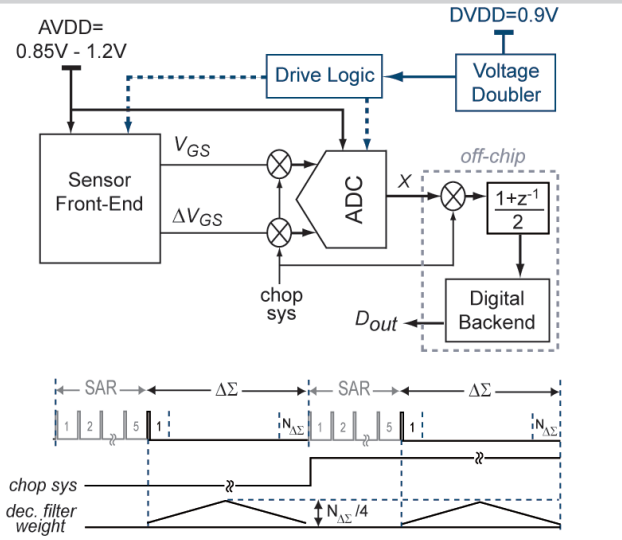

Figure 12.7.2: Top: the sensor's block diagram. Bottom: timing diagram of a temperature conversion.

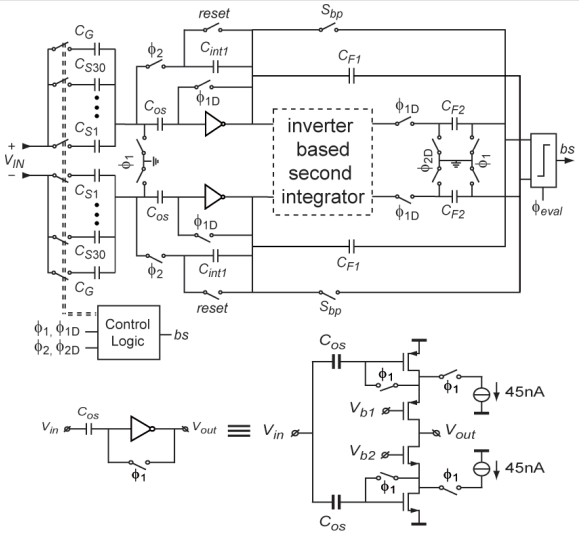

Figure 12.7.3: Top: Circuit diagram of the 2nd-order inverter-based zoom-ADC. Bottom: Circuit diagram of the inverter-based OTA.

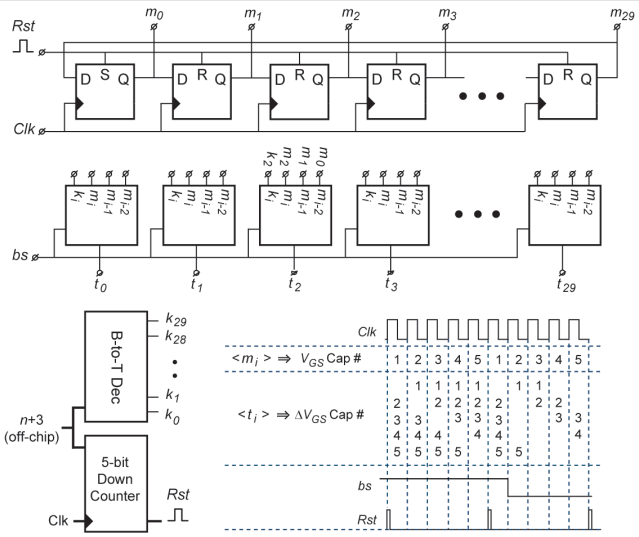

Figure 12.7.4: On-chip DEM logic for the zoom ADC's Cap-DAC (timing is shown for a 5-element Cap-DAC).

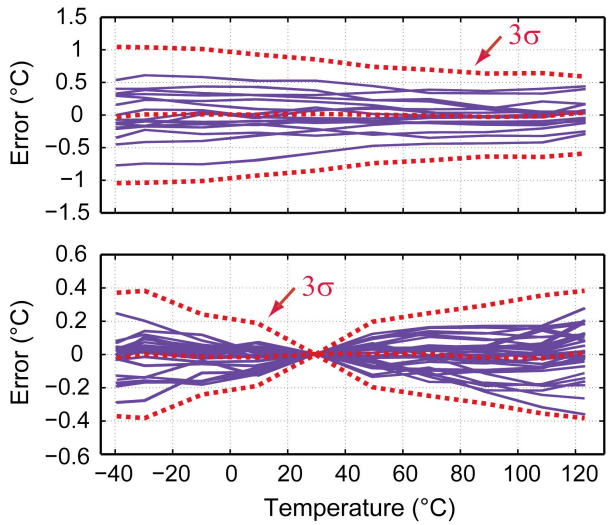

Figure 12.7.5: Measured temperature error of 16 samples after alpha-trimming at 30°C.

Parameter	This work	JSSC'13 [4]	JSSC'10 [5]	CICC'08 [6]	VLSI'11 [7]
Technology	**0.16µm**	0.16µm	0.18µm	0.18µm	0.18µm
Chip area	**0.085mm²**	0.08mm²	0.042mm²	0.05mm²	0.18mm²
Sensor type	**DTMOST**	BJT	MOST	MOST	Resistor
Supply current	**700nA**	3.4µA	190nA	220nA	20µA
Supply voltage	**0.85 - 1.2V**	1.5 - 2.0V	0.5V (sensor) 1.0V (digital)	1V	1.2 - 2V
Supply sensitivity	**0.45°C/V**	0.5°C/V	-	Supply referenced	0.625°C/V
Temperature range	**−40°C to 125°C**	−55°C to 125°C	−10°C to 30°C	0°C to 100°C	0°C to 100°C
Inaccuracy (Trim method)	**±0.4°C[1] (1-point)**	±0.15°C[1] (1-point)	−0.8°C/+1°C[2] (2-point)	−1.6°C/+3°C[2] (2-point)	±0.5°C[2] (1-point)
Relative inaccuracy	**0.48%**	0.2%	4.5%	4.6%	1%
Number of samples	**16**	18	9	5	5
Resolution (T_{conv})	**0.063°C (6msec)**	0.02°C (5.3msec)	0.2°C (30msec)	0.1°C (100msec)	0.25°C (12.5µsec)
Res.FOM	**14.1 pJK²**	11 pJK²	140 pJK²	220 pJK²	19pJK²

1: 3σ, 2: Maximum

Res. FOM=Energy/Conversion× (Resolution)²

Relative inaccuracy(%)=100×Max Error/Specified temperature range

Figure 12.7.6: Performance summary and comparison with previous work.

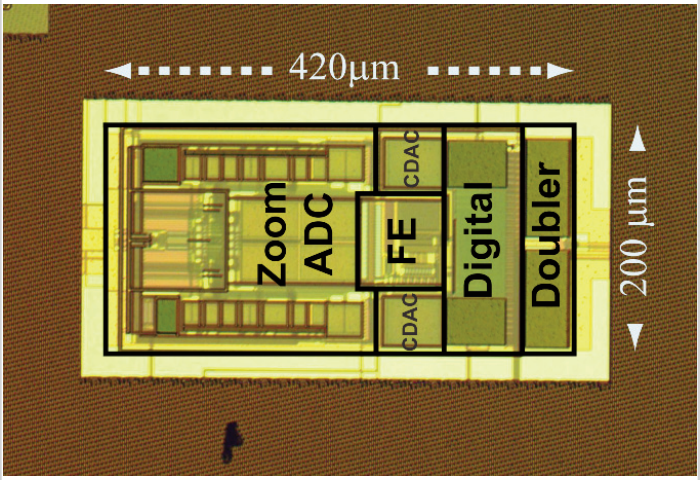

Figure 12.7.7: Chip micrograph of the temperature sensor.

978-1-4799-0920-9/14/$31.00