Thermal Diffusivity Sensing: A New Temperature Sensing Paradigm

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***Abstract*- This paper presents an overview of recently developed absolute temperature sensors based on the measurement of the thermal diffusivity of silicon, *D*. Such sensors make use of the fact that, in IC-grade silicon, *D* has a well-defined temperature dependence and is insensitive to process spread. *D* can be determined by measuring the thermal delay between an on-chip heater and an on-chip relative temperature sensor This delay can then be digitized or used to define the output frequency of an oscillator.**

Proof-of-concept thermal diffusivity (TD) sensors were fabricated in 0.7µm and 0.18µm bulk CMOS, and in 0.5µm SOI technology. Their outputs are well-defined functions of temperature and they work over a wide temperature range from –70°C to 170°C. It was found that the inaccuracy of TD sensors scales with process technology and is insensitive to mechanical stress. An implementation in 0.18µm bulk CMOS achieved an untrimmed inaccuracy of ±0.2°C (3σ) from –55°C to 125°C.

I. Introduction

Over the last few decades, the use of integrated temperature sensors for temperature control and thermal management has become widespread [1]. Because of their low cost and ease of use, CMOS temperature sensors are found in many consumer and industrial applications. Most CMOS temperature sensors are based on the well-understood temperature dependence of bipolar transistors or diodes. However, process spread limits the untrimmed inaccuracy of such sensors to a few degrees Celsius. After batch calibration, the inaccuracy of such sensors can be reduced to ±0.25°C (3σ) over the military temperature range (–55 to 125°C) [2], which can be improved to ±0.1°C (3σ) by individual trimming at a single temperature [3]. However, individual trimming of packaged devices is costly and time-consuming. Wafer level trimming is easier, although the mechanical stress associated with packaging can cause BJT-based sensors to exhibit several tenths of a degree of 'packaging shift' [4]. Moreover, compared to older designs [2], the inaccuracy of BJT-based sensors in deep sub-micron CMOS, at best, has not improved [5][6][7]. Although some recent work has been done on MOSFET-based sensors, their inaccuracy is much worse than that of BJT-based sensors: inaccuracies of –0.4/+0.6°C over a 100°C range have been reported after (costly) two-temperature trimming [8].

A promising alternative is based on the measurement of the thermal diffusivity of bulk silicon, *D*, which is a strong function of absolute temperature *T*, being approximately proportional to $1/T^{1.8}$ [9][10]. *D* can be determined by measuring the time it takes for a small amount of heat to diffuse from an on-chip heater to a neighboring relative temperature sensor, usually a thermopile (Fig. 1). Such a structure is known as an electrothermal filter (ETF), since the heat signal will be delayed and attenuated as it diffuses through the substrate. For highly pure IC-grade silicon, *D* is very well-defined. Furthermore, the spacing between the heater and the thermopile, *s*, is accurately determined by lithography. As a result, thermal diffusivity (TD) sensors have well-defined characteristics and can achieve low untrimmed inaccuracy.

TD sensing was first reported in the 1960's and 70's [11][12], but poor lithography and the lack of precision readout circuitry limited their accuracy. Also, the small signals (millivolts) associated with the high thermal conductivity of silicon resulted in poor resolution [13][14], even when a large amount of heater power (>10mW) was dissipated.

This paper presents an overview of several recently developed temperature-to-frequency and temperature-to-digital converters [15-25] based on the measurement of *D*. Section II discusses the ETF in more detail, after which section III will present several readout architectures that have enabled the development of high-precision TD sensors. Key improvements include significant power reduction, direct digitization and full, CMOS-compatible integration. As will be shown in the measurement results (section IV), these improvements, in turn, have enabled accurate characterization of the effects of lithographic error (for several process nodes), mechanical stress, doping variations and batch-to-batch spread. Measurements on TD sensors, implemented in 0.7µm and 0.18µm bulk CMOS and 0.5µm SOI CMOS technology, show that they indeed have well-defined characteristics and can achieve untrimmed inaccuracies as low as ±0.2°C (3σ) over the military temperature range.

Some potential applications of TD sensors are discussed in section V. Because their inaccuracy scales with process technology, they are well-suited for the thermal management of microprocessors. They can also be used for high-temperature applications (>200ºC), since they are unaffected by leakage currents. The paper ends with conclusions.

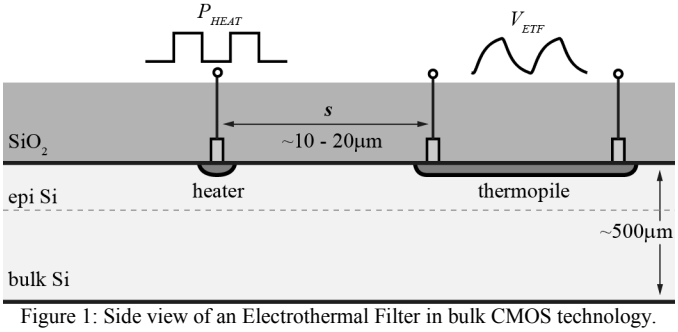

Figure 1: Side view of an Electrothermal Filter in bulk CMOS technology.

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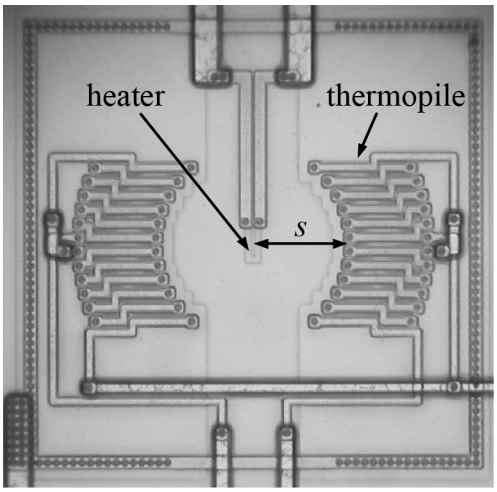

Figure 2: Micrograph showing a CMOS Electrothermal Filter (ETF).

II. The Electrothermal Filter

As discussed in the introduction, D can be determined by measuring the characteristics of an electrothermal filter (ETF). Fig. 2 shows a micrograph of an implementation in a 0.7µm CMOS process. The heater is an n^+-diffusion resistor, while the relative temperature sensor is a thermopile made by connecting a number of p^+-diffusion/aluminum thermocouples in series. This ETF only requires diffusion resistors and interconnect, and so can be implemented in any CMOS process.

Since D is finite and temperature-dependent, an ETF can be seen as a thermal low-pass filter with *temperature-dependent* filtering characteristics. Its phase shift will then be a function of absolute temperature and, advantageously, be immune to amplitude variations caused by the effect of process spread on heater resistance and thermopile sensitivity.

The simplest possible ETF consists of a point heater and a point sensor at the surface of an infinitely thick substrate. If the generated heat is a sine wave with frequency f_{ETF} then it can be shown [26] that the phase shift ϕ_{ETF} of the sensor's output is given by:

$$\phi_{ETF} \propto s\sqrt{\frac{f_{ETF}}{D(T)}} \qquad (1)$$

So if either f_{ETF} or ϕ_{ETF} is constant, the other variable will be a function of temperature. Simulation results for f_{ETF} = 85kHz or ϕ_{ETF} = 90° are shown in Fig. 3, under the assumption that s = 24µm and D(300K) = 0.89cm/s^2. From (1), it follows that in constant phase mode, $f_{ETF}(T) \propto 1/T^{1.8}$, and that in constant frequency mode, $\phi_{ETF}(T) \propto T^{0.9}$. The effect of thermal expansion on s is at the 3ppm/K level, and can be neglected.

More complex ETF geometries (such as the ETF in Fig. 2) can be made to approximate the point ETF model by locating the junctions of the thermopile on the heater's constant phase-shift contours [19]. This strategy maximizes the ETF output voltage (V_{ETF}), since it maximizes the vector sum of the individual thermocouple voltages.

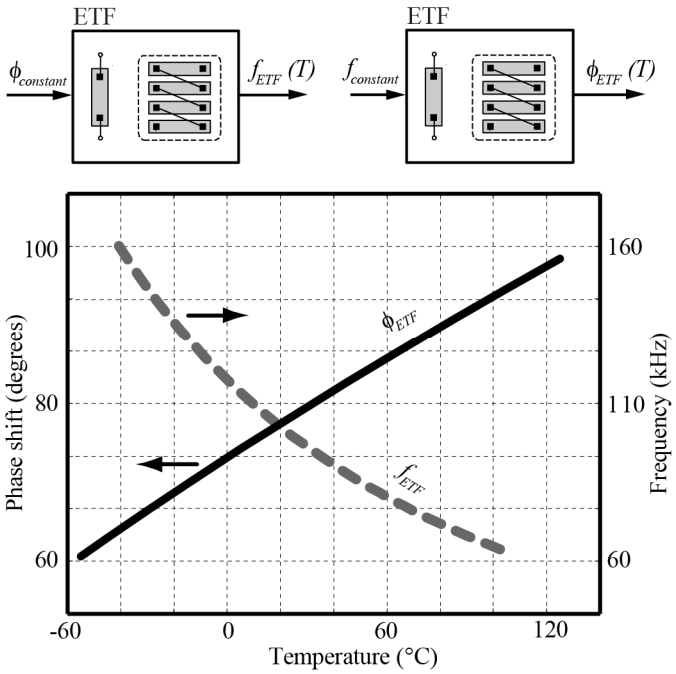

Figure 3: Temperature-dependent ETF output characteristics for both phase- and frequency readout.

The accuracy of an ETF depends on the accuracy of its geometry and of D. For IC-grade silicon, and low doping levels (less than 10^{17} atoms/cm^3), D is insensitive to process spread [18][25][27]. Two important geometric parameters are the location of the heater and the location of the thermopile's hot junctions. Errors in the former are rejected by the ETF's circular symmetry (Fig. 2), while the latter is defined by the contact mask. Lithographic inaccuracy ($\delta s/s$) is the dominant source of error in ETFs, and, for a given technology, can be minimized by making s sufficiently large.

The main challenge associated with reading out an ETF is obtaining sufficient SNR. For the Fig. 2 ETF, a heater power dissipation (P_{heat}) of 1mW, a thermopile sensitivity of 10mV/K and s = 24µm, V_{ETF} is typically only 160µV$_{pp}$. The white noise associated with the thermopile's resistance (several kΩ) then dictates a narrow readout bandwidth. For P_{heat} = 1mW and a noise bandwidth of 1Hz, the noise level will be only 0.19°C$_{rms}$ [21]. This is rather high; BJT-based temperature sensors typically require only tens of µW's for similar noise performance.

One way to improve the ETF's SNR is by moving the thermopile closer to the heater, i.e. by reducing s. A scaled version of the Fig. 2 ETF (s=11µm), in the same process, had 3.3x more SNR. However, the relative effect of lithographic error increases linearly, increasing the untrimmed temperature inaccuracy.

ETFs can also be implemented in SOI technology, in which case the buried SiO_2 layer will reduce the amount of heat lost to the substrate, thereby increasing V_{ETF} (Fig. 4). FEM simulations show that the presence of a SiO_2 layer (buried at a depth of a few microns) increases V_{ETF} (and therefore the SNR) by about 5x. In an SOI process, an ETF with s = 24µm was measured to have a noise level of 0.037°C$_{rms}$ (again for P_{heat} = 1mW and a 1Hz noise bandwidth) [25].

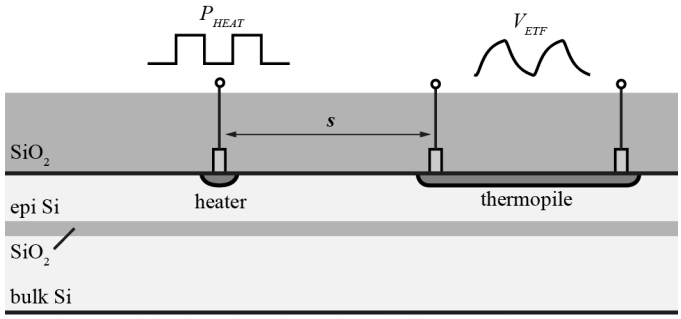

Figure 4: Side view of an Electrothermal Filter (ETF) in SOI CMOS. The buried SiO_2 layer reduces the amount of heat lost to the substrate.

III. ETF Readout Architectures

From the SNR discussion above, it is clear that successful ETF readout architectures must be narrowband systems, and that their resolution will probably be thermal-noise limited. Since the output of an ETF is a phase-shifted AC signal, this suggests the use of synchronous phase detection.

An example of such a readout architecture is the electrothermal frequency-locked loop (FLL), shown in Fig. 5. Here the ETF is driven by a voltage-controlled oscillator (VCO), while its phase shift ϕ_{ETF} is detected by a synchronous phase detector that drives an integrator. The VCO's output frequency is adjusted until the integrator's DC input becomes zero. This corresponds to a 90° phase shift between its two inputs, and so ϕ_{ETF} is forced to 90°. From (1), this ensures that $f_{VCO}(T) \propto 1/T^{1.8}$. Furthermore, the presence of an integrator reduces the system bandwidth to a narrow band around f_{vco}. This architecture has been successfully used to demonstrate the feasibility of TD sensing [15-19].

In many applications, however, a digital output is preferred. This can be obtained by driving the ETF at a constant frequency, f_{drive}, derived from a frequency reference such as a crystal oscillator. From (1), this ensures that $\phi_{ETF}(T) \propto T^{0.9}$, which can then be digitized with respect to the fixed f_{drive} .

Fig. 6 shows a precision phase-digitizer. Once again, the ETF's output signal is multiplied by a phase-shifted copy of f_{drive}, such that the integrator DC input becomes zero. However, the phase-shifted signal is now generated by a digital phase rotator driven by an n-bit ADC. The output of the ADC will then be a digital approximation of ϕ_{ETF} [20].

By regarding the phase-rotator as a phase-domain DAC, and the synchronous phase-detector as a phase differencing node, the system of Fig. 6 may be seen to be an n-bit 1st-order, phase-domain sigma-delta modulator (PDΣΔM). Since the required bandwidth is rather low, the sampling frequency can be chosen high enough to ensure that the modulator's resolution is not limited by quantization noise, even when a single-bit phase DAC is used.

Fig. 7 shows an implementation of a 1st order, single-bit PDΣΔM [20]. The integrator and multiplier are implemented by a g_m-C stage and chopper, respectively. The modulator's output bitstream is the weighted average of two reference phase shifts, ϕ_0 and ϕ_1, which also define the PDΣΔM's phase input range. Since the phase detector is no longer operated at zero DC output, a cosine non-linearity is introduced.

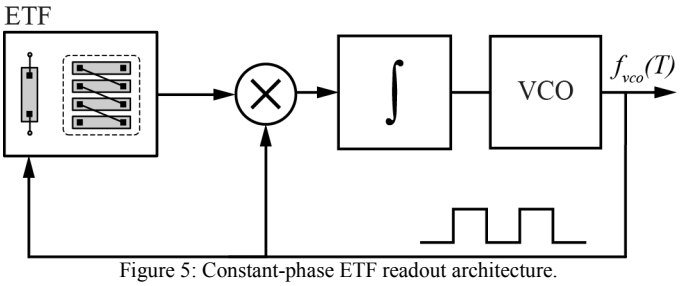

Figure 5: Constant-phase ETF readout architecture.

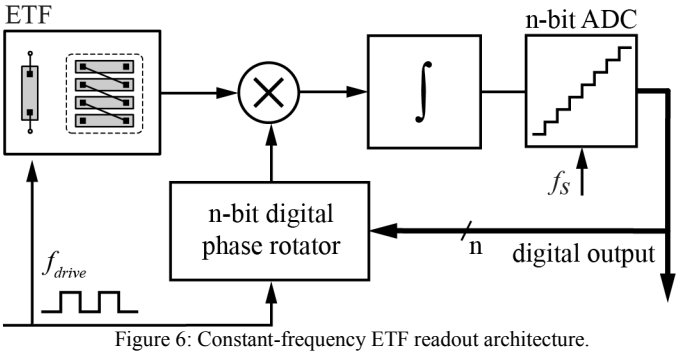

Figure 6: Constant-frequency ETF readout architecture.

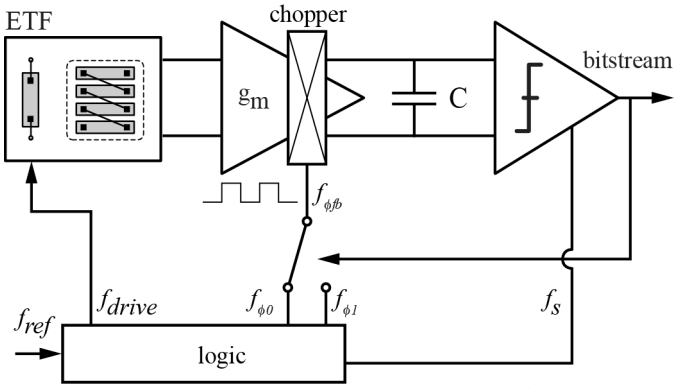

Figure 7: An ETF interfaced by a phase-domain sigma-delta modulator.

However, this nonlinearity is systematic and can either be removed by digital post-processing, or used to compensate the $T^{0.9}$ nonlinearity of ϕ_{ETF} [23].

System-level chopping (not shown) is used to accurately process the ETF's sub-millivolt output signals, while the modulator's decimation filter defines the noise bandwidth. Using this architecture, fully integrated PDΣΔMs with the 14 to 16-bit phase resolution required for precision temperature sensing have been realized [21][24].

IV. Measurement Results

A. Implementations

To investigate the feasibility of TD sensing, several test devices have been fabricated. The results of implementations at three different technology nodes (0.7µm and 0.18µm CMOS, and 0.5µm SOI) will be discussed here. A chip photo of a 0.18µm CMOS test device is shown in Fig. 8. All the results presented were achieved with the PDΣΔM-based readout architecture discussed above, and, unless otherwise noted, all the devices were packaged in ceramic DIL packages.

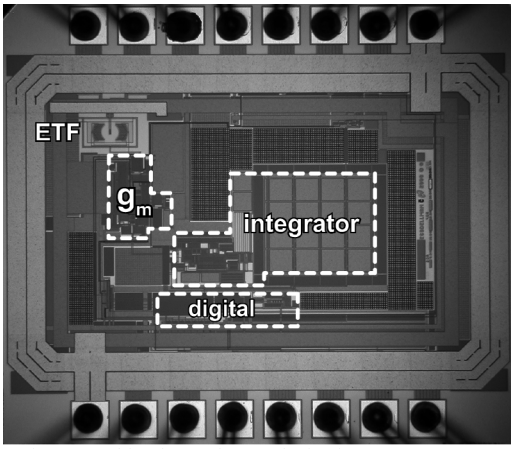

Figure 8: Chip photo of a test device in 0.18µm CMOS.

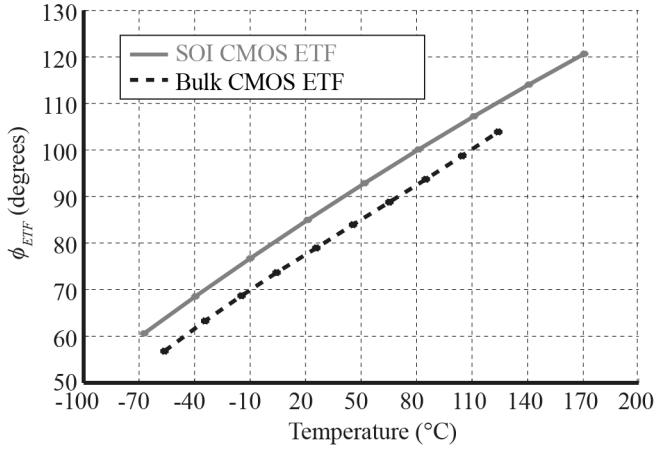

Figure 9: Measured ϕ_{ETF} as a function of temperature.

B. ETF Characteristics

Fig. 9 shows the decimated output of the PDΣΔM as a function of temperature for realizations of the reference ETF (Fig. 2) in both bulk and SOI CMOS. It can be seen that in both cases, ϕ_{ETF} has the expected $T^{0.9}$ temperature dependence up to at least 170°C. Compared to bulk CMOS, the buried SiO_2 layer of the SOI realization increases the thermal impedance between the ETF's heater and thermopile, and thus causes a systematic increase in $\phi_{ETF}(T)$.

C. Device-to-device spread

The device-to-device spread of a TD sensor in a given process is determined with respect to a master curve that represents the average $\phi_{ETF}(T)$ for a given ETF. Measurements on 16 devices in 0.7µm CMOS show that the resulting spread of the reference ETF corresponds to an untrimmed temperature error of ±0.6°C (3σ) from –55°C to 125°C [21]. When implemented in 0.18µm CMOS, the same ETF has an untrimmed inaccuracy of only ±0.2°C (3σ) over that same range (Fig. 10) [24]. These results demonstrate that the device-to-device spread is indeed a strong function of the lithographic accuracy of the process. Measurements on another 16 devices, packaged in plastic TSSOP packages, show that they follow the same master curve, but exhibit slightly increased spread (±0.3°C).

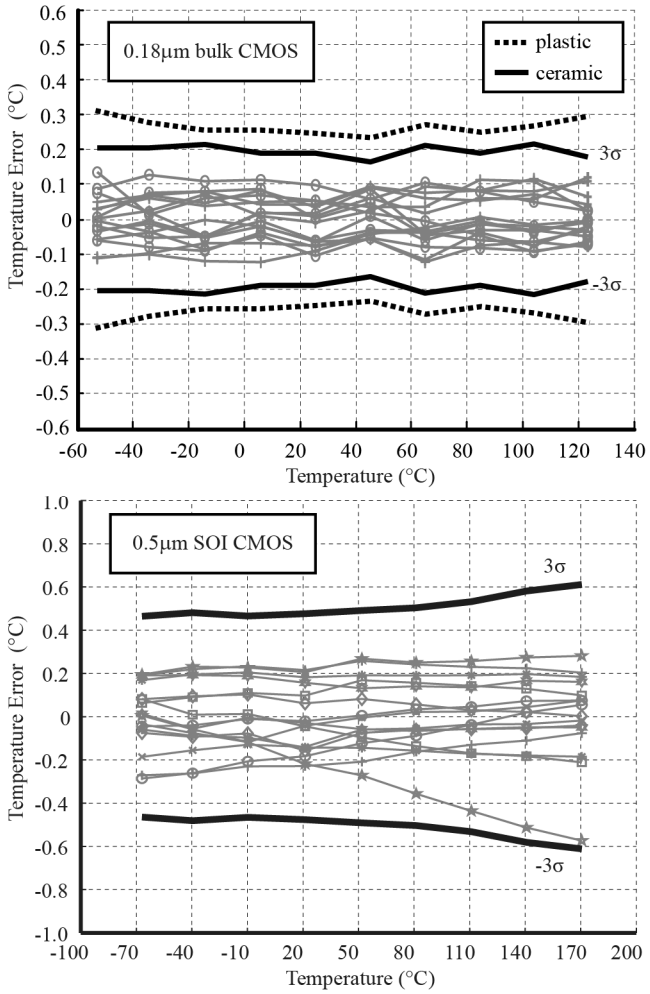

Figure 10: Measured device-to-device spread in bulk and SOI CMOS. The black lines indicate 3σ limits.

This result demonstrates that ETFs, unlike BJTs, do not suffer from packaging shift. The slight increase in spread was attributed to the larger thermal resistance (~100K/W) of plastic packages, which increases the amount of self-heating. Variations in either the thermal resistance of the package or the TD sensor's power consumption (~3mW) result in variations in self-heating, and thus increased spread.

As shown in Fig. 9, the SOI devices were measured over an extended temperature range (–70°C to 170°C). Over this range, their untrimmed inaccuracy was ±0.6°C (3σ) [25], which is in line with the expected lithographic inaccuracy of the process.

D. Batch-to-Batch Spread

Rather surprisingly, since lithography was thought to be the dominant source of error, measurements on devices from two MPW runs in 0.18µm CMOS showed significant batch-to batch spread. As shown in Fig. 11, the devices exhibited a batch-to-batch offset of about 2°C, while the intra-batch spread remained at ±0.2°C (3σ). In SOI, however, the batch-to-batch variations are much smaller, and a worst case shift in average of about 0.2°C was observed, based on 3 MPW runs over a 1 year period.

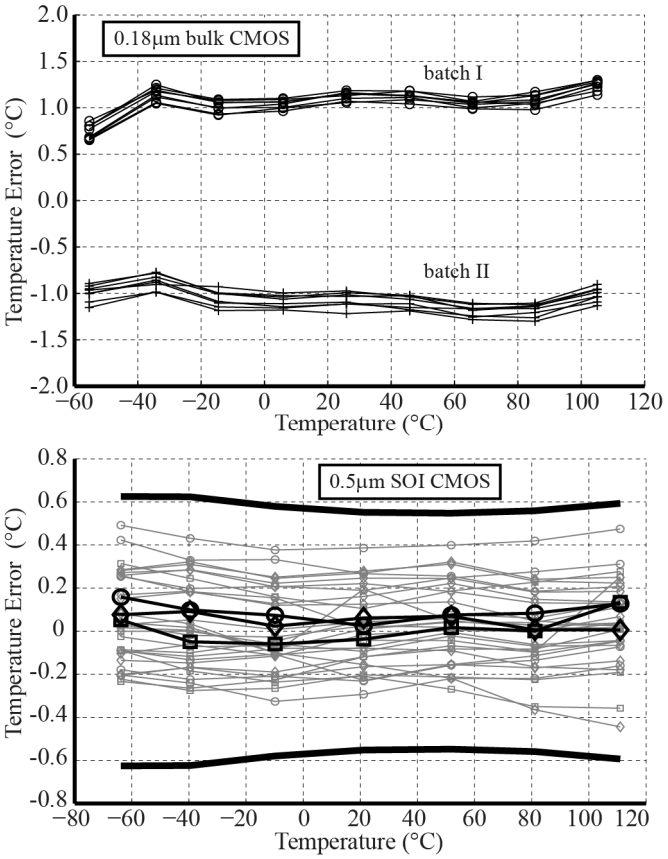

Figure 11: Batch-to-batch spread data for ETFs in 0.18µm CMOS (2 batches) and 0.5µm SOI (3 batches). The middle bold lines in the lower plot indicate batch averages.

The most likely cause for the observed batch-to-batch offset is a combination of spread in the thickness of the lightly-doped epi-layer and spread in the doping level of the heavily doped p^+-substrate. It is known that the thermal conductivity of heavily doped silicon is about 20–30% lower than that of lightly-doped silicon [27]. Since the epi-layer is typically only a few microns thick while s = 24µm, the reference ETF will be sensitive to both the thickness of the epi-layer and the doping level of the substrate [28]. This hypothesis is strengthened by the measurements in SOI CMOS, since the presence of the thermally insulating buried oxide ensures that heat diffusion in the ETF is dominated by the well-defined diffusivity of the lightly-doped epi-layer.

By applying a batch offset trim to the bulk CMOS devices, the residual batch-to-batch error can again be reduced to ±0.2°C over a –15°C to 125°C range. At lower temperatures, this error increases to ±0.6°C.

E. Thermal interference

When used in ASICs, other heat sources on the die may potentially interfere with the temperature variations detected by the ETF's thermopile. Because the readout circuit is based on synchronous detection, this is only a problems if the heat is generated at f_{drive} (or its odd multiples), and only if the source of interference is close to the thermopiles, since its heat output would otherwise be thermally low-pass filtered by the die.

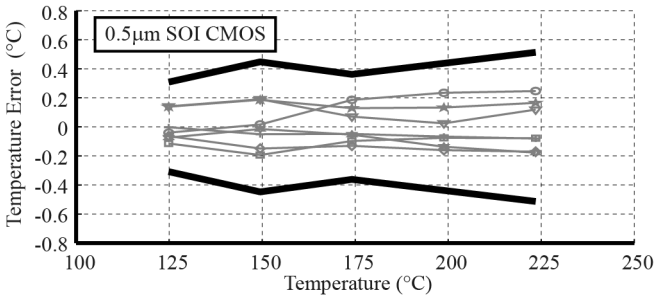

Figure 12: Device-to-device spread for 8 devices measured at high temperatures.

The ETF's sensitivity to interference was tested by driving a neighboring heater located 120µm away with a 12mW pseudo-random heat signal derived from f_{drive}. While an increased self-heating of about 0.5°C was measured, the ETF's resolution or its inaccuracy did not degrade, demonstrating that most of the thermal interference was indeed filtered by the thermal inertia of the die [20].

V. Applications

A. High temperature sensing

There is an increasing need for temperature sensing at high temperatures (>125ºC) in industrial and automotive applications. However, recently released commercial BJT-based sensors offer only ±1.0ºC inaccuracy at 175ºC [29][30]. Because D is a monotonic function of temperature over a very wide temperature range [9][10] and because leakage current is only a second-order effect for thermal *delay*-based temperature sensors [22], TD sensors maintain their low untrimmed inaccuracy at even higher temperatures. Preliminary measurements on a few samples indicate that untrimmed inaccuracies of ±0.5ºC (3σ) up to 225ºC are possible (Fig. 12).

B. Thermal management of microprocessors

Thermal management of multi-core microprocessors and other large SoCs typically requires several tens of temperature sensors, since large temperature gradients and local hotspots can occur [31]. Although such sensors typically require only moderate accuracy, trimming is undesirable, and they may only occupy minimal chip area [7]. TD sensors are highly aligned with these requirements, since they offer low untrimmed inaccuracy and their area scales with process technology. For the required temperature range (50ºC to 120ºC), the intra-batch variations are expected to be low, while inter-batch variations can be corrected by a simple wafer-level offset trim.

Thermal management also requires high conversion rates [7], to accommodate the large thermal transients that occur when large digital blocks, e.g. individual microprocessor cores, are switched on and off. Extrapolating from the current measurement results [24], an ETF with s = 2µm will achieve an untrimmed inaccuracy of ±0.5ºC (3σ) when implemented at the 32nm node. A heater power consumption of 500µW would then yield 0.2ºC_{rms} resolution at a 1kS/s conversion rate. In SOI processes, even less power consumption will be

required. Compared to BJT-based sensors in such processes [5][7], TD sensors should achieve better untrimmed accuracy and smaller area, at comparable power dissipation and resolution.

C. Frequency references

Apart from temperature sensing, ETFs have also been used to create fully integrated frequency references [32]. These also exploit the well-defined characteristics of D, but compensate for its temperature dependence; an inaccuracy of ±0.1% from –55ºC to 125ºC has been achieved.

VI. Conclusion

This work has presented an overview of temperature sensors based on the measurement of the temperature-dependent thermal diffusivity of silicon (TD sensing). Because this physical property is well-defined, sensors with low untrimmed inaccuracy can be fabricated. The performance of TD sensors scales with process technology and they are insensitive to packaging stress. A 0.18µm CMOS device offers an untrimmed inaccuracy of ±0.2°C (3σ) over the military temperature range, while another device in 0.5µm SOI CMOS offers an untrimmed inaccuracy of ±0.6°C (3σ) from –70°C to 170°C, and low (~0.2°C) batch-to-batch variations. Their wide operating range makes thermal diffusivity sensors well suited for industrial and automotive applications, while their scaling properties promise greatly improved performance in deep submicron CMOS, making them an interesting alternative to less accurate BJT-based temperature sensors.

Acknowledgments

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